

What is claimed is:

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1. A test circuit for inclusion on an integrated circuit comprising:  
a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and  
a data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier so that said corresponding data verification parameter does not verify data content of said identified data unit.
  2. The test circuit of claim 1 wherein said data verification parameter generator inverts a data verification parameter generated from said data content of said selected data unit.
  3. The test circuit of claim 1 wherein said data verification parameter generator inverts a portion of said data content of said selected data unit that is used to generate a data verification parameter.
  4. The test circuit of claim 1 wherein said data identifier identifies a data group and said data verification parameter corresponds to said identified data group.

5. The test circuit of claim 1 wherein said data identifier uses data content to identify said data unit.

6. The test circuit of claim 1 wherein said data identifier uses data unit position to identify said data unit.

7. A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:

identifying a data unit other than a next data unit to be transferred in a data sequence; and

generating an erroneous data verification parameter that does not verify data content of said identified data unit.

8. The method of claim 5 wherein said generation of said erroneous data verification parameter includes inversion of a data verification parameter generated from said data content of said selected data unit.

9. The method of claim 5 wherein said generation of said erroneous data verification parameter includes inversion of a portion of said data content of said selected data unit that is used to generate a data verification parameter.

